AMENDMENTS TO THE SPECIFICATION

Applicants respectfully present the following amendments to the specification.

Please amend the paragraph beginning on line 1 of page 2 as follows:

In the construction of Fig. 1, a pair of bit lines BL and /BL are connected to a sense amplifier 11. The amplification function of the sense amplifier 11 amplifies and holds a differential potential appearing between the bit lines BL and /BL. Each of the bit lines BL and /BL are coupled to memory cells, each of which includes a transistor 12 driven by a word-line potential and a memory cell capacitor 13 for storing data as electric charge. Word lines wl00 through wl(n) correspond to respective word addresses. Each of the bit lines BL and /BL is connected to a single dummy cell. The dummy cell includes a transistor 14 driven by a dummy word line (dwl0C, dwl01), a dummy cell capacitor 15 for storing data as electric charge, and a transistor 16 for precharging the dummy cell capacitor 15. When the transistor 16 becomes conductive by a dummy cell precharging line dcp, a potential vdc is supplied to the dummy cell capacitor 15.

Please amend the paragraph beginning on line 24 of page 2 as follows:

A bit line bl (collectively representing both of the bit lines BL and /BL) is precharged to a power-supply potential, for example. At timing t1, the dummy cell precharging line dcp is set to HIGH to disconnect the dummy cell capacitor 15 from the potential vdc, thereby finishing precharging of the data-storage node of the dummy cell. At timing t2, the dummy word line dwl is activated (changed to LOW) so as to change

the potential of one of the bit lines according to the potential of the dummy cell capacitor 15. At timing t3, the word line ~~2l~~ wl is activated (changed to LOW) so as to change the potential of the other bit line according to the potential of the memory cell capacitor 13. Timing t2 and timing t3 may be reversed in order, or may be simultaneous. The sense amplifier 11 amplifies a minute potential difference between the bit lines, thereby sending the data.

Please amend the paragraph beginning on line 12 of page 13 as follows:

A semiconductor memory device [[20A]] 20B of Fig. [[7]] 9 includes a refresh timer 36, which replaces the memory cell refresh timer 31 and the dummy cell refresh timer 32 by combining their functions in the semiconductor memory device 20 of the first embodiment shown in Fig. 4. Further, the memory cell address counter 33 and the dummy cell address counter 34 are consolidated into an address counter 37.

Please amend the paragraph beginning on line 34 of page 13 as follows:

The address counter 37 of Fig. 10 includes a plurality of counter circuits 61 connected in a cascade series, with the counter circuit 61 at the top receiving the instruction signal EN from the refresh timer 36. The outputs of the counter circuits 61 obtained in parallel are supplied as a refresh address. The refresh address is counted up one by one each time the instruction signal EN is input. In this configuration, the low-order (l+1) bits rf<0> through rf<1> represent a word line selecting address WL select Address, and the high–order [[(j-1)]] (j-l) bits rf<l+1> through rf<j> represent a block selecting address Block select Address. Namely, a shift to the next block is made

when the refresh operation is completed with respect to all the word addresses in a given block by refreshing word lines one after another. In the next block, word lines will then be refreshed one after another.

Please amend the paragraph beginning on line 16 of page 14 as follows:

The address counter 37 of Fig. 11 includes the counter circuits 61 connected in cascade series as in the construction of Fig. 10, with the outputs of the counter circuits 61 being obtained in parallel as a refresh address. In this configuration, however, the low-order [[(j-1)]] (j-l) bits rf<l+1> through rf<j> represent a ~~word line~~ block selecting address Block select Address, and the high-order (l+1) bits rf<0> through rf<1> represent a ~~block~~ word line selecting address WL select Address. In this configuration, thus, a shift to the next block is made when a given word address is refreshed in a given block, followed by the same word address being refreshed in the next block. This is repeated until the same word address is refreshed in all the blocks. Then, a return to the first block is made, and the next word address is refreshed from the first block to the last block, which is then repeated.

Please amend the paragraph beginning on line 5 of page 17 as follows:

The flip-flops 89 through 93 are set by corresponding ones of the pulse signals $\phi 1$ through $\phi 8$, and are reset by other ones of the pulse signals $\phi 1$ through $\phi 8$. As a result, the flip-flops 89 through 93 generate a bit-line-precharge-control-timing signal [[t_bus]] 1 bts (no precharge during the HIGH period), a word-line-control-timing signal [[t]] 1_wl (activation of word lines during the HIGH period), a dummy-word-line-control-

timing signal [[t]] 1_dwl (activation of dummy word lines during the HIGH period), a dummy-cell-precharge-control-timing signal [[t]] 1_dcp (precharge during the HIGH period), and a sense-amplifier-control-timing signal [[t]] 1_le (activation of sense amplifiers during the HIGH period), respectively. Based on these signals, the precharging of memory cells (or read operations) and the precharging of dummy cells are performed in a similar manner as shown in the operation timing of Fig. 3. With this provision, the present invention controls the precharging of dummy cells to finish it after a predetermined time period, thereby achieving a constant time length of precharging of dummy cells regardless of long or short access intervals. This achieves a stable read operation.

AMENDMENTS TO THE DRAWINGS

Applicants respectfully present herewith replacement Figures 2, 3, 4, 6, 10 and 11 which include the desired changes and which comply with 37 C.F.R. §1.84(p)(5). The changes made to Figures 2, 3, 4, 6, 10 and 11 are explained in the accompanying remarks section below.